

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
20 June 2002 (20.06.2002)

PCT

(10) International Publication Number
WO 02/49110 A1

(51) International Patent Classification⁷: **H01L 27/04**,
23/60, 23/64

NORSTRÖM, Hans [SE/SE]; Mårdstigen 3, S-170 71
Solna (SE). CARLSSON, Mats [SE/SE]; Vallstigen 22,
S-174 46 Sunbyberg (SE).

(21) International Application Number: PCT/SE01/02768

(74) Agent: **BERGENSTRÄHLE & LINDVALL AB**; Box
17704, S-118 93 Stockholm (SE).

(22) International Filing Date:
13 December 2001 (13.12.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
0004614-4 13 December 2000 (13.12.2000) SE

(81) Designated States (*national*): AE, AG, AL, AM, AT, AU,
AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ,
DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR,
HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR,
LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ,
NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK,
SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA,
ZM, ZW.

(71) Applicant (*for all designated States except US*): **TELE-
FONAKTIEBOLAGET L M ERICSSON (PUBL)**
[SE/SE]; S-125 26 Stockholm (SE).

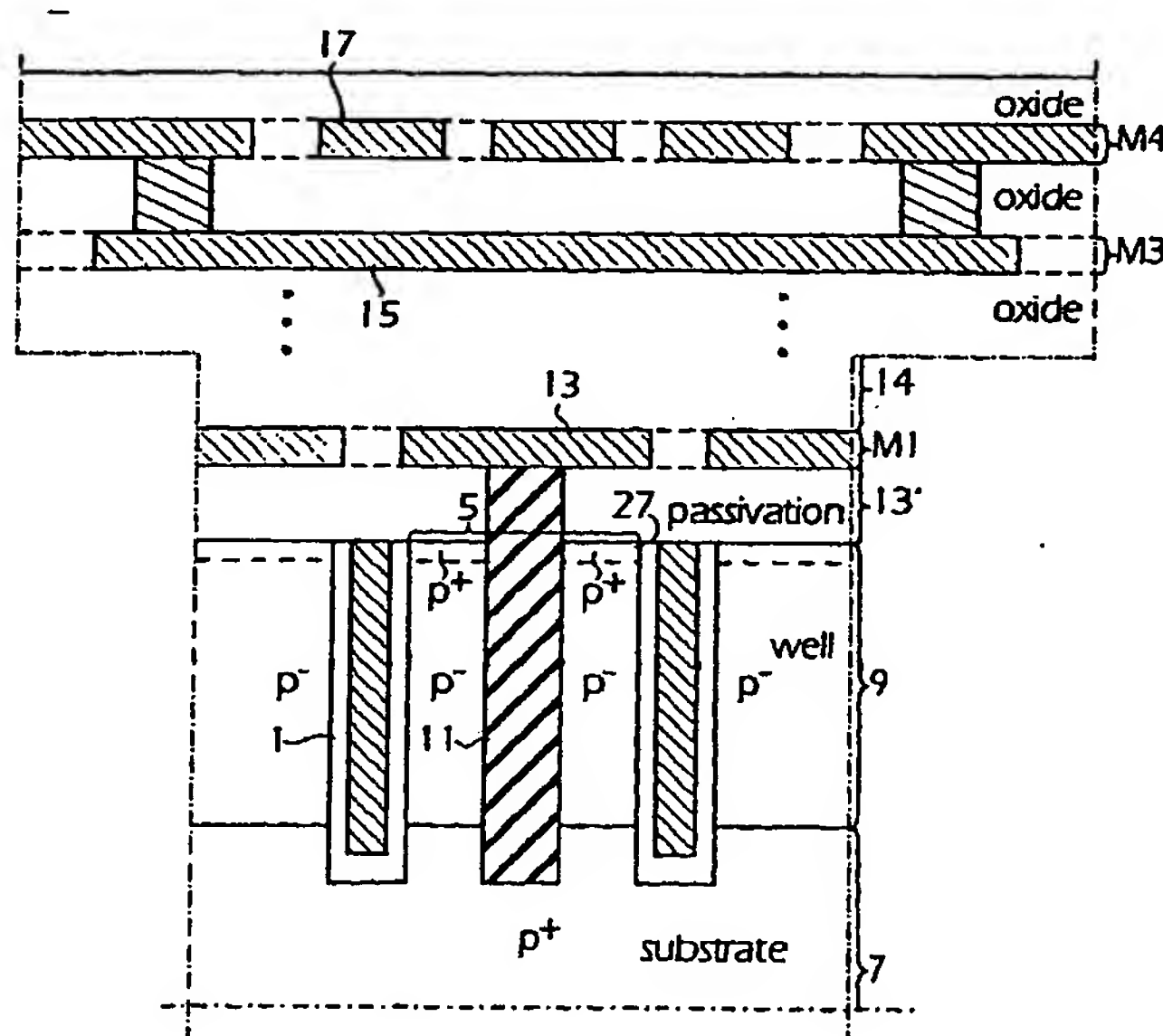
(84) Designated States (*regional*): ARIPO patent (GH, GM,
KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW),
Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM),
European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR,
GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent
(BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR,
NE, SN, TD, TG).

(72) Inventors; and

(75) Inventors/Applicants (*for US only*): **JOHANSSON**,
Ted [SE/SE]; Sveavägen 66, S-182 62 Djursholm (SE).

[Continued on next page]

(54) Title: SHIELDED INDUCTOR



(57) Abstract: An integrated circuit comprises an inductor path (17) formed in a metal layer located in a surface structure on top of an electrically well conducting substrate (7). Trenches (1) filled with an electrically isolating material are located under the inductor path and are arranged in a meshlike or grid pattern. In order to improve the shielding of the inductor path and to simultaneously improve the Q-value of the inductor, in the islands (5) of material formed in the surface structure between the meshes of the pattern deep substrate contacts (11) are located. The substrate contacts extend down into the substrate and the substrate and the contacts are intended to be connected to ground potential. Electrically conducting areas (13) can cover the islands and are then connected to the substrate contacts.



Published:

— with international search report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

SHIELDED INDUCTOR

TECHNICAL FIELD

The present invention relates to a shielded inductor for an integrated circuit and an integrated circuit having a shielded inductor.

BACKGROUND

5 Silicon bipolar, CMOS and BiCMOS integrated circuits are all used today for high-speed application in the frequency range of 1 - 3 GHz, replacing circuits which could previously only be made using methods including materials of the groups III and V of the periodic system. Inductor elements are often needed in high-frequency circuit building blocks such as resonators and filters. A problem common to all integrated circuits is how
10 to achieve inductors having sufficiently high quality factors or Q-values, and sufficiently high operating frequencies which obviously are limited by the resonance frequencies.

Recent advances in processing silicon for producing integrated circuits have allowed inductor layouts having a higher inductance per unit area and lower losses owing to reduction of feature sizes and multilayer metallization structures including thick oxide
15 assisting in isolating the inductors from the substrate. Still, there remain considerable losses due to the resistivity of the metallization layers, the electrical coupling to the substrate and losses in the substrate. Thus, it is difficult to obtain inductor elements of say the 2 - 10 nH range having Q-values higher than 10 in the 1 - 2 GHz frequency range when producing electronic integrated circuits based on silicon.

20 Integrated inductors are usually given layouts comprising square or octagonal metal stripes configured as spiral. Because of the electrically conducting properties of the silicon substrate, the Q-values are reduced. By selectively removing the silicon under the conductor forming the inductor, higher Q-values and higher self-resonant frequencies can be obtained. Thus, the Q-values can be increased by a factor of two by such a removal, as
25 disclosed in J.Y.-C. Chang, A.A. Abidi, M. Gaitan, "Large Suspended Inductor on Silicon and Their Use in a 2 μ m CMOS RF Amplifier", Trans. El. Dev., Vol. 14, No. 5, p. 246, May 1993, and U.S. patent 5,539,241 for Abidi et al. The removal can be made by etching the silicon producing air gaps of several hundreds of μ m, but such methods are not regarded to be feasible in larger production volumes or to be compatible with normal pro-
30 cessing flows used in producing integrated circuits on silicon.

In C.P. Yue, S.S. Wong, "On-Chip Spiral Inductors with Patterned Ground Shields for Si-Based RF IC's", J. Solid-State Circuits, Vol. 33, No. 5, p 743, May 1998 and in the published International patent application WO 98/50956, inventors C.P. Yue, S.S. Wong, is disclosed that a patterned ground shield layer is placed under the inductor and
35 above the semiconductor substrate. This design results in improved Q-values owing to both a shielding effect against inducing electrical currents in the substrate and a reduction of the induced eddy currents in the ground shield because the ground shield is patterned in such a way that the currents cannot circulate in the metal below the inductor, see Figs. 1a, 1b of this application.

40 In Burghartz et al., "Progress in RF Inductors on Silicon - Understanding MMIC

Inductors", IEDM Tech. Digest, 1998, pp. 523 - 526, a comparison of different methods of reducing substrate losses, among these the structures described in the cited article by C.P. Yue et al. and in cited patent application having Yue et al. as inventors, is made.

The research field of inductors integrated in silicon structures is still in progress. Reported results may appear to contradict each other. The exact mechanisms of the losses and the best way of modelling the structures by equivalent circuits, describing the production of losses in a physical, not too simplified way are still discussed. An inductor structure having good characteristics when used in one application circuit will sometimes have not as good characteristics when used in a circuit of a different kind, i.e. the electric behaviour of the inductor structure depends on the actual circuit or more particularly on the exact physical surrounding structure. Therefore, it is difficult to determine the optimum structure of an inductor by only theoretical investigations or calculations.

The method described in the article by C.P. Yue et al. and in the corresponding patent improves the performance of inductors. However, the metallization pattern must be continuous and must be connected to a fixed potential at some point, preferably at several points, in order to operate well as a shield. However, no means are provided to improve the effect of the substrate under the metallization pattern. Also, the pattern has openings towards the substrate in which the electromagnetic field can penetrate. According to our experiments and the cited article by Burghartz et al., grounding the substrate close to the electrical conductor constituting the inductor can improve the Q-value, because a highly electrically conductive substrate having a well-defined potential such as the ground potential also serves as a shielding and reduces the effects of eddy currents in the silicon. However, in processes actually used to fabricate integrated circuits, there is no quite good front-side contact. Those which are used still have considerable electrical resistances to the substrate.

In the published International patent application WO 97/35344 corresponding to U.S. patent application 08/821,880, "Semiconductor device shielded by an array of electrically conductive pins and a method to manufacture such a device", inventors Tomas Jarstad and Hans Norström, a shielding of a semiconductor component or conductor path on a semiconductor substrate is disclosed, the shielding comprising separate substrate contacts arranged in a pattern around the component or path, each contact having a relatively small cross-sectional area and the cross-sections e.g. being squares.

Furthermore, in the published Japanese patent application 11-145386 an inductor is disclosed which has a trench extending in parallel to the electrical conductor path of the inductor and located in the between adjacent portions of the spiral conductor path. In U.S. patent 5,742,091 for Francois Hébert an inductor structure having a spiral metal conductor is disclosed, in which a continuous deep trench is located directly underneath the spiral path. Also, a second continuous spiral trench can be arranged in the interspaces between the first trench, i.e. also between adjacent portions of the spiral conductor. In an alternative embodiment the trench has a mesh-like rectangular pattern located underneath all of the area occupied by the conductor and can be considered as consisting of two sets of

intersecting trench segments, the segments in each set being parallel to each other. In U.S. patent 5,717,243 an inductor structure having a spiral metal conductor is disclosed, in which radial trenches under the spiral path are arranged.

In the published International patent application WO 97/45873 corresponding to U.S. patent application 08/865,130, "Conductors for integrated circuits", inventors Ted Johansson and Hans Norström, an inductor structure having a spiral metal conductor is disclosed, in which a mesh-like pattern of trenches are located underneath the area occupied by the metal conductor. The pattern can be a rectangular pattern consisting of two sets of intersecting trenches, the trenches in each set being parallel to each other.

10 SUMMARY

It is an object of the present invention to provide an inductor structure for an integrated circuit having an improved electrical shielding.

It is another object of the present invention to provide an inductor in an integrated circuit having an improved Q-value.

15 A problem which the invention intends to solve is thus generally how to improve the Q-value of an inductor included in an integrated circuit. In particular the problem is how to shield the parasitic capacitances derived from the substrate without degrading the inductance of such an inductor.

Thus generally, a shielded inductor comprises an electrical conductor configured in a 20 suitable way, such as in a spiral pattern, and a large array of trenches, formed in a pattern under the electrical conductor. The islands between the openings of the trenches contain the silicon substrate and an epitaxial structure formed on top of a substrate. The substrate is well conducting and can have weakly or poorly doped layer on top of it. The trenches extend from the surface down to the layer having a doping of p+ or n+. In the islands 25 substrate contacts are arranged connected to metal areas covering the upper surface of islands, one separate metal area provided for each substrate contact. The metal areas are thus laterally separated from each other and they can cover substantially all of the surface of the islands and preferably also extending a little over the adjacent trenches, over small marginal regions thereof.

30 Additional objects and advantages of the invention will be set forth in the description which follows, and in part will be obvious from the description, or may be learned by practice of the invention. The objects and advantages of the invention may be realized and obtained by means of the methods, processes, instrumentalities and combinations particularly pointed out in the appended claims.

35 BRIEF DESCRIPTION OF THE DRAWINGS

While the novel features of the invention are set forth with particularly in the appended claims, a complete understanding of the invention, both as to organization and content, and of the above and other features thereof may be gained from and the invention will be better appreciated from a consideration of the following detailed description of non- 40 limiting embodiments presented hereinbelow with reference to the accompanying drawings,

in which:

- Fig. 1a is a perspective view of a patterned ground shielding according to prior art,
- Fig. 1b is a top view of a rectangular spiral inductor placed over the patterned ground shielding of Fig. 1a according to prior art,
- 5 - Fig. 2a is a schematic cross-sectional view of a portion of an integrated circuit showing a surface structure including an inductor path having a shielding configured in an alternative way,
- Fig. 2b is a schematic view from above of the portion of the shielding shown in Fig. 2a,
- Fig. 2c is a schematic view from above of an inductor placed above the surface structure
- 10 of Figs. 2a and 2b,
- Fig. 3 is a view from above of a trench pattern used under an inductor of an integrated circuit according to prior art,
- Fig. 4a is a schematic cross-sectional view of a portion of an integrated circuit showing a surface structure including an inductor path having an additional shielding structure,
- 15 - Fig. 4b is a schematic view from above of the portion of the shielding shown in Fig. 4a, and
- Fig. 5 is a schematic view from above of an inductor path surrounded by a frame.

DETAILED DESCRIPTION

Fig. 3 is a view from above of a portion of a substrate in which a large array of
20 trenches 1 has been etched to form some suitable pattern. The trench pattern is used under a shielded inductor for reducing losses of the inductor to the substrate, as suggested in the cited U.S. patent for Hébert and the cited International patent application WO 97/45873. The pattern shown comprises a first set of several straight identical trenches located in parallel to each other and having an equal spacing and also a second set of identical
25 trenches located in parallel to each other and equally spaced, the trenches of the second set being perpendicular to those of the first set. In any pattern chosen the trenches should be so long and so located that they pass beyond the outermost turn of the inductor into the material of the substrate surrounding the inductor. The trench pattern used can have any meshlike shape, including interconnected short trench segments delimiting relatively small
30 islands which are separated from each other. The islands can accordingly have any suitable preferably convex shape such as triangular, square, rectangular, rhombic, hexagonal, octagonal, circular, etc. The trenches are generally deep elongated, continuous recesses or grooves extending from some surface layer of the structure down into the substrate.

The islands 5 between the trenches are remaining portions of a silicon substrate or
35 substrate layer 7 and of some layer structure formed on top of the substrate, see the schematic cross-sectional view of Fig. 2a. The substrate 7 has doping type p+ or n+ and thus has a relatively good electrical conductivity and in the embodiment shown, on top of it a weakly doped well layer 9 of doping type p- or n- is located. The trenches 1 extend from the surface of the p- or n-well layer 9 down into the substrate or layer 7 having a good
40 electrical conductivity by the doping of type p+ or n+. The doping types of the substrate

7 and the well are in the embodiment shown in Fig. 2a equal, i.e. they are both p-type or n-type, but they could also be different, i.e. the substrate can be p-type and the well n-type or the substrate can be n-type and the well p-type.

In each island 5 remaining between the trenches 1 a substrate contact or contact pin 11 made from a suitable filling, electrically conductive material such as a metal like W is located, e.g. of the type disclosed in the cited International patent application WO 97/35344. These contact pins 11 can be connected to metal areas 13 placed on top of each remaining island 5 and extend into the substrate layer 7, to which it is thus electrically connected and which is intended to be connected to some constant potential like a ground potential, thereby shielding the substrate from the electrical field generated by the electrical current flowing in the electrical conductor path of the inductor. Thus, only the electrical field is blocked what results in a smaller influence on the inductor by the parasitic capacitances. The magnetic field is not blocked. For a whole shielding having no holes the magnetic field would be blocked and thereby the inductance and the Q-value of the considered inductor reduced. The substrate contacts 11 have generally the shape of narrow pins or rods formed in deep blind-holes in the well 9 extending into the substrate layer 7. The pins or rods can suitably have a square cross-section.

The metal areas 13 are formed as separate islands over the remaining silicon in each island 5 and extend up to the edges of the trenches 1 forming the boundaries of the respective islands and also preferably extend some small distance past these boundaries, thus having narrow marginal strips located above the trenches 1. The metal areas 13 are through the substrate contacts 11 and the substrate 7 electrically connected to a ground potential. They are not in direct contact with any other metal area, as seen in the view from above in Fig. 2b. Thereby, eddy currents induced in the metal areas 13 are reduced.

The metal areas 13 can be remaining regions of a patterned first metal main layer M1 in or at the surface of the structure, this first metal layer being formed on top of a passivation layer 13' in turn located directly on top of the well 9 and the trenches 1. On top of the structure illustrated in Fig. 2b and having a top metal layer M1 another normal passivation layer or electrically isolating layer 14 is deposited, such as a silicon oxide layer. Further patterned metal main layers M2, M3, ... can be provided on top of the isolating layer 14. The further metal main layers are then also patterned and they are separated by electrically isolating layers, e.g. of silicon oxide. In these layers the spiral conductor path of an inductor is fabricated using the further metal layers as is well-known in the art, see e.g. the cited International patent applications. Thus, in a lower metal layer such as M3 a bottom connector path 15 can be formed and in the metal layer M4 directly on top thereof the very inductor path 17 can be formed, see also Fig. 2c showing the final structure as seen from above. In this figure a region 19 is seen that is located under all of the inductor path and is completely filled with an array of trenches and substrate contacts as described with reference to Figs. 2a and 2b.

The whole of the inductor structure can be surrounded by a frame 21 constituted of

regions of the same metal layer as the metal areas 13, see Fig. 2b and Fig. 5. The metal frame 21 is electrically connected to an underlying frame-like configuration of rows of contact pins 23 made in the same way as the substrate contacts 11 and penetrating into the substrate 7. The metal frame 21 is a continuous strip having a gap or opening 25 to make it
5 an open structure in order to avoid circulating currents.

Typical values can be that the trenches have a width of $1\ \mu\text{m}$, the islands have dimensions of $3.5 \times 3.5\ \mu\text{m}^2$ and the metal islands $3.7 \times 3.7\ \mu\text{m}^2$.

The design described above comprising isolated metal islands reduces losses derived from the silicon substrate. Thus, it will improve the Q-values of the inductors.
10 Furthermore, no additional processing steps are generally required provided that substrate contacts according to the disclosure of the published International patent application PCT/SE97/00487 corresponding to U.S. patent application 08/821,880 are used.

To further enhance the effect of the highly conductive, grounded substrate 7, if required, an additional doping of type p+ or n+ respectively, extending from the surface
15 of the well layer 9 and some distance into this layer, can be used, see the regions 27 in Fig. 2a. These additional doped regions can be obtained by ion implantation and are the same doping type as the well 9. Together with the substrate contact pins 11 they work as surface-to-substrate contacts.

To further improve the shielding of the substrate as described in the article for C.P.
20 Yue et al. and in International patent application WO 98/50956 cited above, regions 29 of an additional electrically conducting, patterned layer which have a substantially inverted location in relation to the metal islands 13 described above and having some overlap can be placed over or under the shielding islands 13, as illustrated by the schematic cross-sectional view of Fig. 4a and the top view of Fig. 4b. The regions 29 can be formed in a second
25 metal main layer M2 and thus have a configuration substantially agreeing with that of the trenches 1, however, the paths thereof can obviously be somewhat wider or narrower than the trenches. These regions of the additional conducting patterned layer can be typically connected to a ground potential.

The main steps of a method of fabricating the structure illustrated in Figs. 2a - 2c
30 will now be briefly described.

First, some substrate or substrate layer 7 is provided which has a good electrical conductivity and thus is heavily doped, to either p+ as shown or n+. The well layer 9 is then applied on top of the substrate such as by epitaxial growth. It is medium doped to have a rather low electrical conductivity, to doping type p- in the example shown but can
35 equally well be doped to n-. Thereupon, deep and narrow recesses or voids for the trenches are produced by first applying a mask and then dry etching to make recesses extending into the surface of the substrate layer 7. The mask layer is removed and the recesses are refilled with an electrically isolating material like silicon oxide, undoped polysilicon or another dielectric material, and in any case the material should have a lower
40 electrical conductivity than the electrical conductivity of the substrate layer 7 and of the

well layer 9. For sufficiently narrow grooves the surface above the substrate produced in the refilling process will be substantially flat. The trenches 1 thus produced can have widths of about 1 - 2 μm and depths of about 5 - 20 μm . The width of the surface structure and substrate material between neighbouring trenches may be as small as is practically possible, for instance in the range of 2 - 4 μm .

If desired, an additional doping to produce the regions 27, see Fig. 2a, intended for improved shielding and consisting of additionally implanted dopants of the same doping type as the well 9, may be made at this stage, using a patterned photomask to only implant areas inside the inductor structure to be formed.

10 On the wafer surface, about 1 μm of electrically isolating material, preferably silicon dioxide, is deposited, and may be subsequently planarized using conventional methods to form the isolating layer 13'. Next, a mask layer for deep holes is applied to the substantially flat surface of the isolating material and then patterned. The mask windows and the deep holes to be produced can have dimensions corresponding to the width of the
15 trenches, i.e. they can have widths/diameters in the range of 1 - 2 μm . The deep holes are produced by dry-etching and the mask layer is removed. The deep holes are in the etching procedure given a depth larger than the height of the isolating layer 13' and the well layer 9 to reach down to the highly doped substrate 7. Thereupon conventional contact holes, not shown, down to any active or passive devices, not shown, that need electrical contact are
20 made, and subsequently in all contact holes a bottom metal layer, not shown, is applied, e.g. containing Ti, Pt, Co, not adhering to the top isolating material of the layer 13'. This bottom metal layer is annealed for a short time to form a good metal-semiconductor contact. A barrier metal, not shown, e.g. TiN, is deposited in the holes on top of the bottom metal layer, and finally the holes are filled with CVD-deposited tungsten W, but
25 other metals could also be used to form the substrate contacts 11 and other contact plugs. During the deposition, the deep holes will be completely filled with metal, "plugged", if the deposited thickness is in the same magnitude of order as the transverse dimensions or diameter of the deep holes. During the plugging procedure, tungsten W is also deposited on the wafer surface. Next, another electrically conductive layer, for example comprising
30 aluminum, is deposited all over the wafer surface. After patterning and etching through the two conductive layers using conventional methods, the patterned W and Al stack will serve as the first metal main layer M1.

Another electrically isolating oxide layer 14 is then applied, holes are etched in this layer and on top of this isolating layer another metal layer is applied. This another metal
35 layer (the layer M3 of Fig. 2a) is patterned to include the electrical conductor 15 for connecting the inner end of the inductor path. A further electrically isolating, oxide layer is then applied, holes therein are produced and on top of it a third metal layer (the layer M4 of Fig. 2a) is applied and patterned to form the inductor path 17. The thicknesses of each of the main metal layers can typically be in the range of 1 - 2 μm . The width of the con-
40 ductor path forming the inductor can be about 5 μm and the distance between neighbouring

portions of the path can be the same order of magnitude as the width of the paths. The top metal layers can be produced by depositing a suitable metal material to also fill holes in the oxide layer to make electrical connections to the conductors of the underlying metal layer. After deposition, the metal layers are etched using conventional methods to form the
5 required conductors.

The additional patterned metallization layers (such as M2 of Fig. 4a), if required, are formed by conventional methods, e.g. similar to those described for the top metal layers.

While specific embodiments of the invention have been illustrated and described herein, it is realized that numerous additional advantages, modifications and changes will
10 readily occur to those skilled in the art. Therefore, the invention in its broader aspects is not limited to the specific details, representative devices and illustrated examples shown and described herein. Accordingly, various modifications may be made without departing from the spirit or scope of the general inventive concept as defined by the appended claims and their equivalents. It is therefore to be understood that the appended claims are intended
15 to cover all such modifications and changes as fall within a true spirit and scope of the invention.

CLAIMS

1. An integrated circuit comprising an inductor including a metal conductor formed in a surface structure located on an electrically well conducting substrate, in particular on a doped silicon substrate, and trenches in the surface structure extending down into the substrate, located under the metal conductor and filled with an electrically isolating material, the trenches arranged in a meshlike or grid pattern forming islands of the surface structure and the substrate material between meshes of the pattern between adjacent portions of the trenches, **characterized** by substrate contacts located inside the separate islands formed in the meshes, the substrate contacts made from an electrically conducting material and extending in the surface structure down into the substrate.

2. An integrated circuit according to claim 1, **characterized** by separate first electrically conducting areas covering the islands, the first electrically conducting areas being connected to the respective separate substrate contacts and electrically isolated from each other.

3. An integrated circuit according to claim 2, **characterized in** that the first electrically conducting areas extend to cover relatively narrow marginal portions of the adjacent trenches.

4. An integrated circuit according to claim 2, **characterized in** that the first electrically areas are electrically isolated from the metal conductor by an electrically isolating layer applied on top of the first electrically conducting areas.

5. An integrated circuit according to claim 1, **characterized in** that in the separate islands the material has at its surface a doping to make the surface electrically well conducting.

6. An integrated circuit according to claim 2, **characterized** by second electrically conducting areas covering the trenches.

7. An integrated circuit according to claim 6, **characterized in** that the second electrically conducting areas have substantially the same configuration patterns as the trenches.

8. An integrated circuit according to claim 6, **characterized in** that the second electrically areas are regions of a metallized layer located in a plane above or beneath the first electrically conducting areas.

9. An integrated circuit according to claim 1, **characterized** by a metal frame surrounding the metal conductor of the inductor.

10. An integrated circuit according to claim 9, **characterized in** that the metal frame is electrically connected to a structure of substrate contacts located under the metal frame.

11. An integrated circuit according to claim 9, **characterized in** that the metal frame is a continuous strip having at least one gap.

12. An integrated circuit according to claim 2, **characterized** by a metal frame surrounding the metal conductor of the inductor and made in a metal layer from which the separate first electrically conducting areas are made.

1/4

Fig. 1a

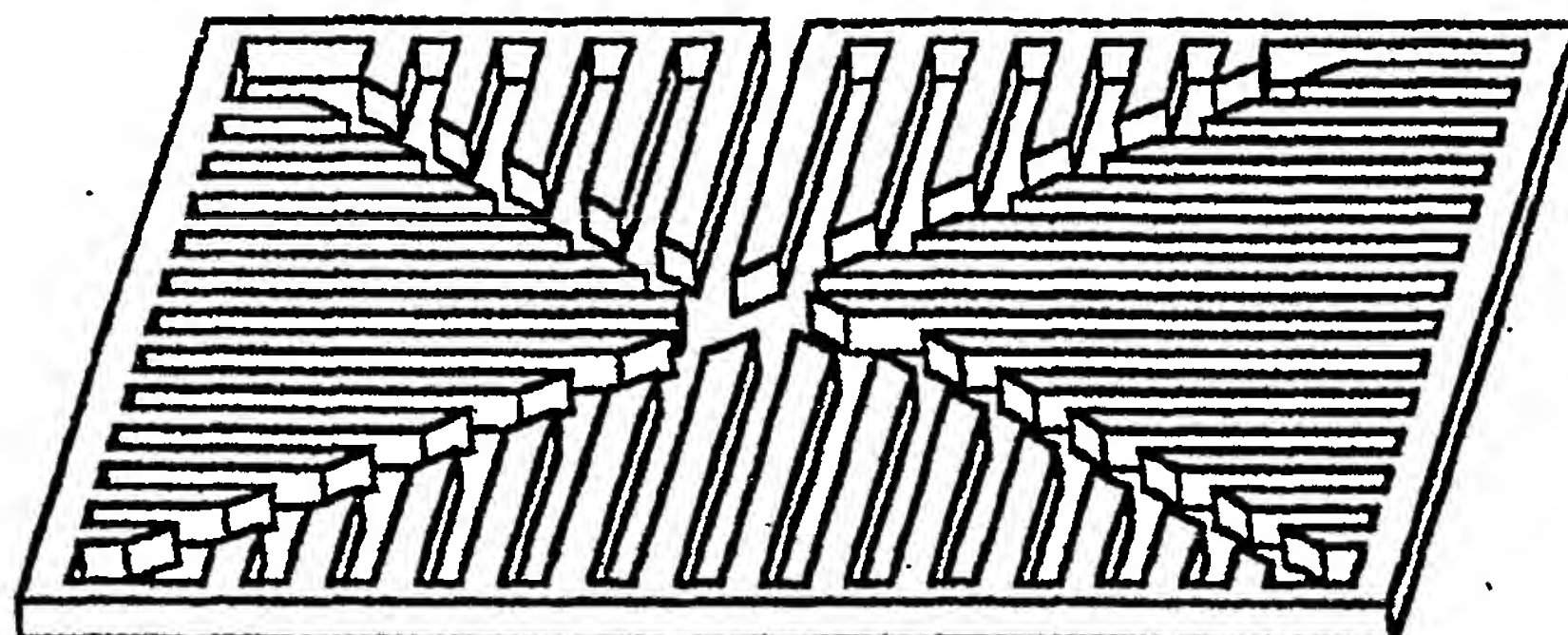
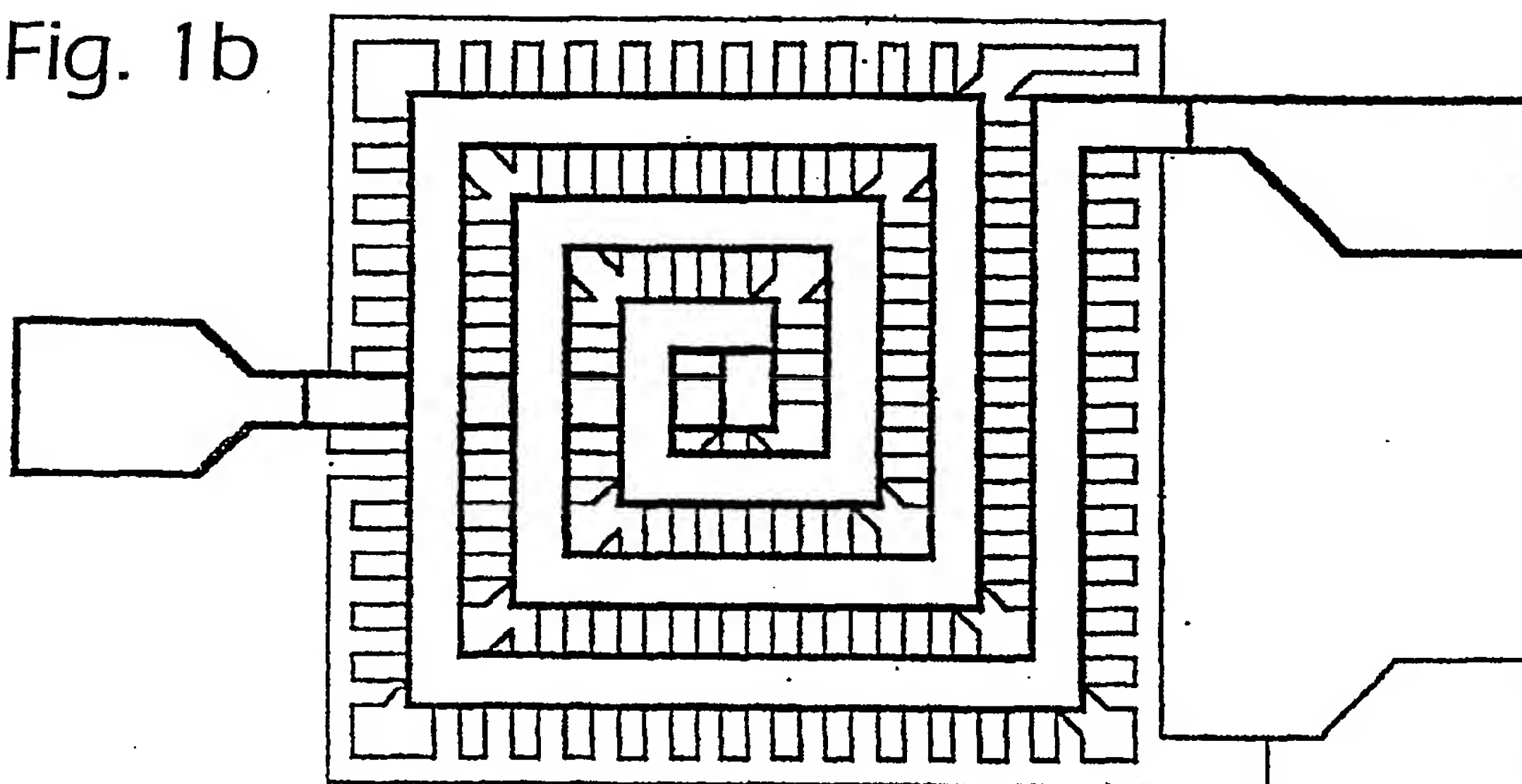


Fig. 1b



2/4

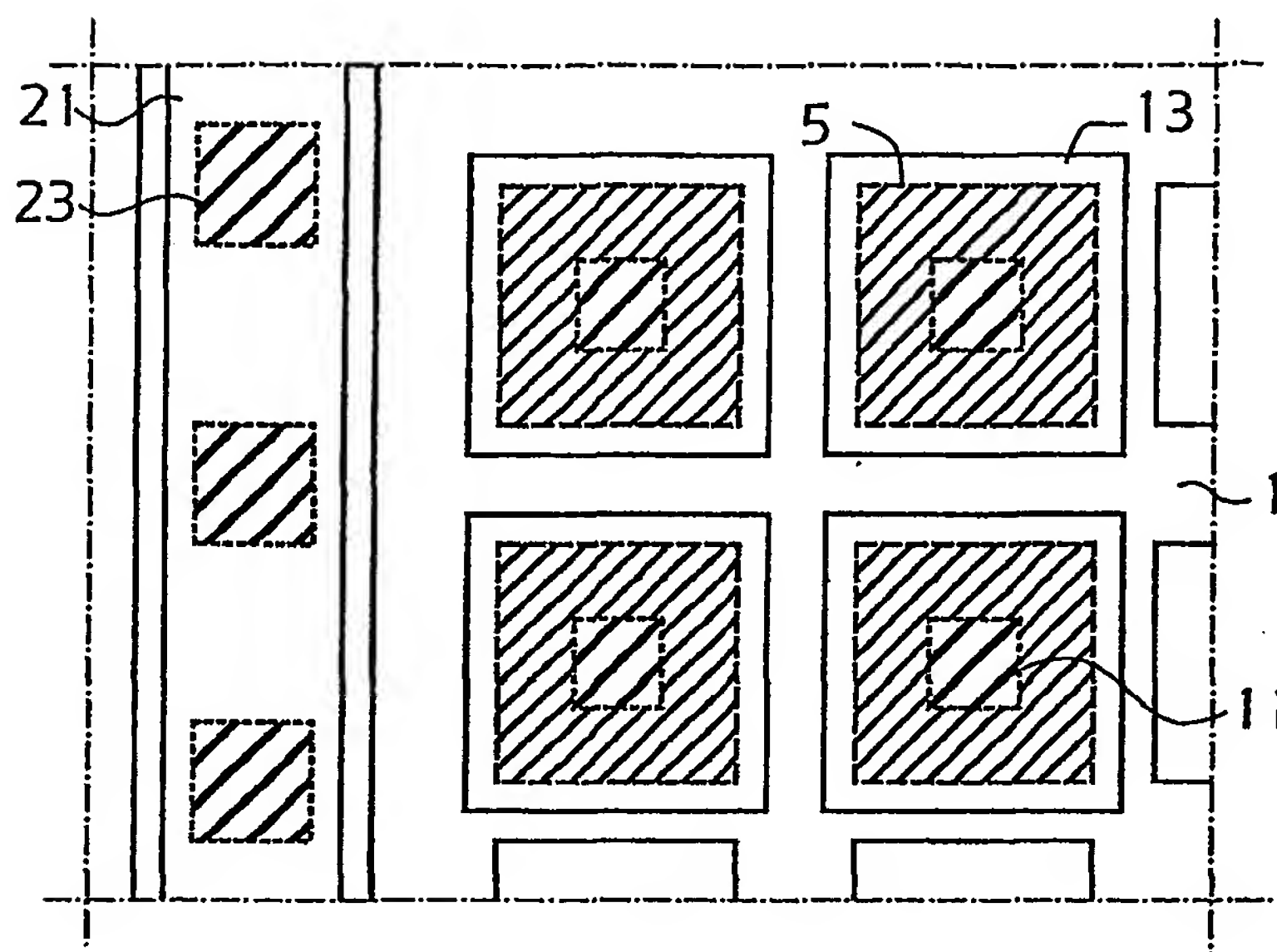
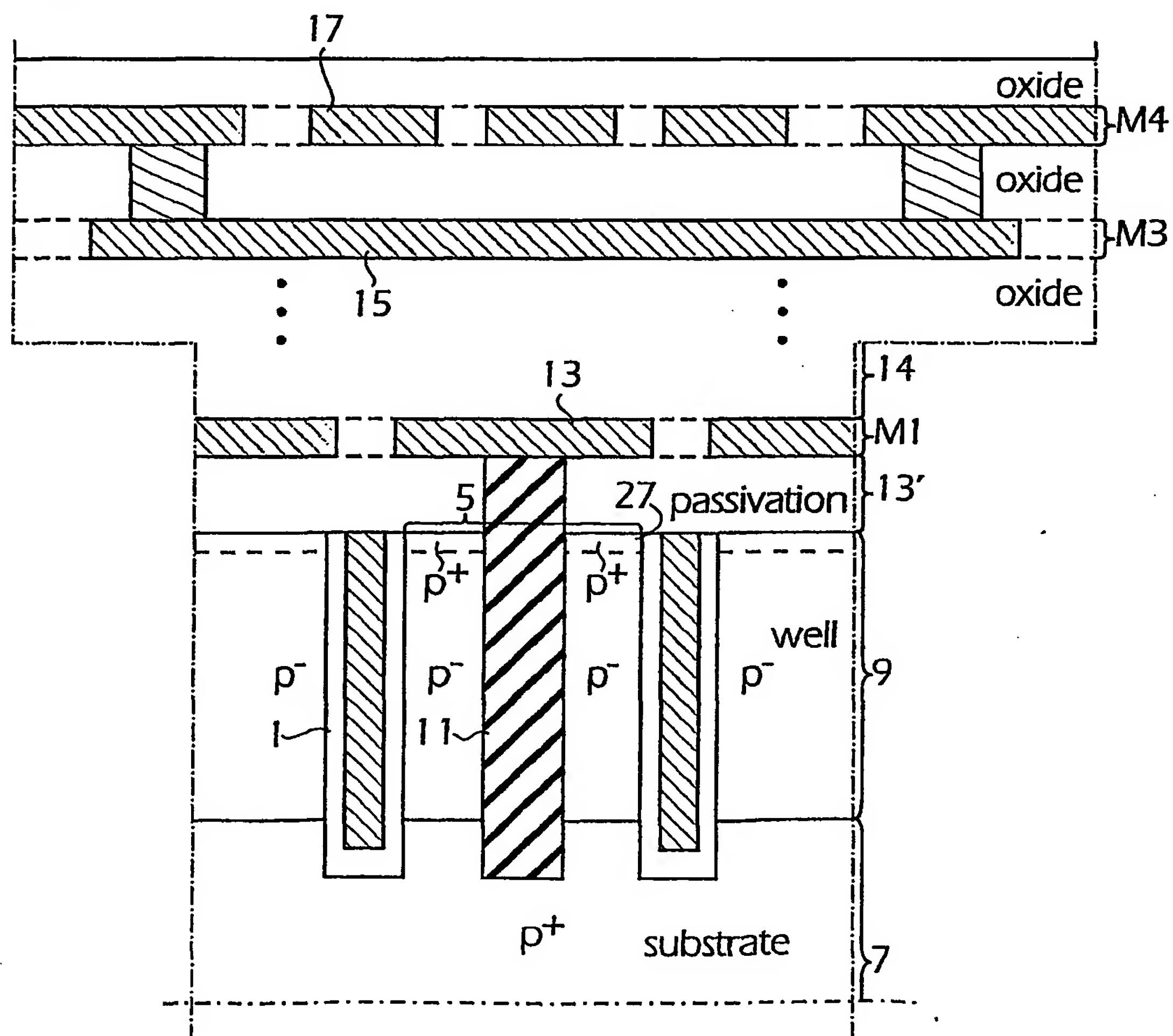
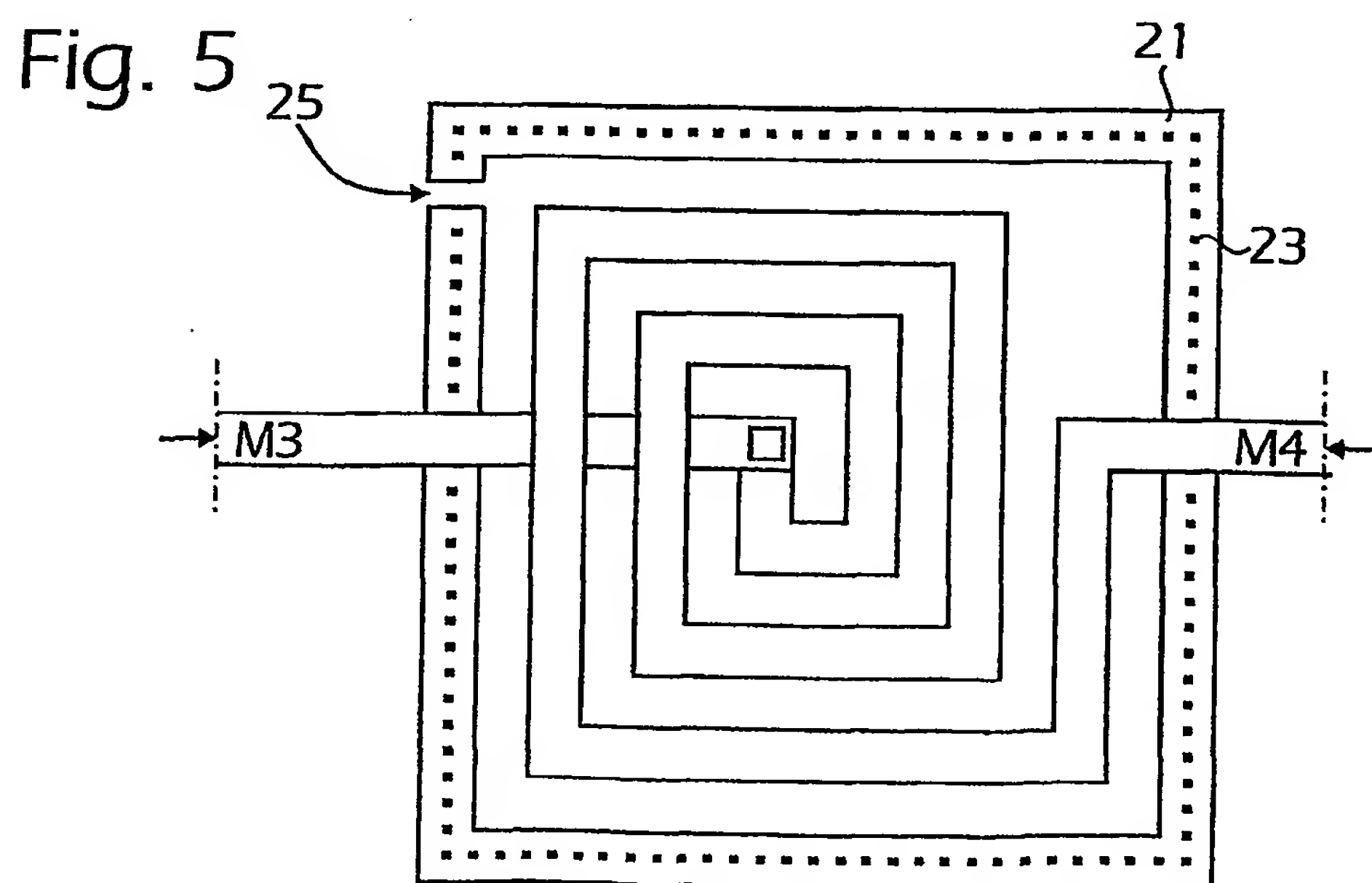
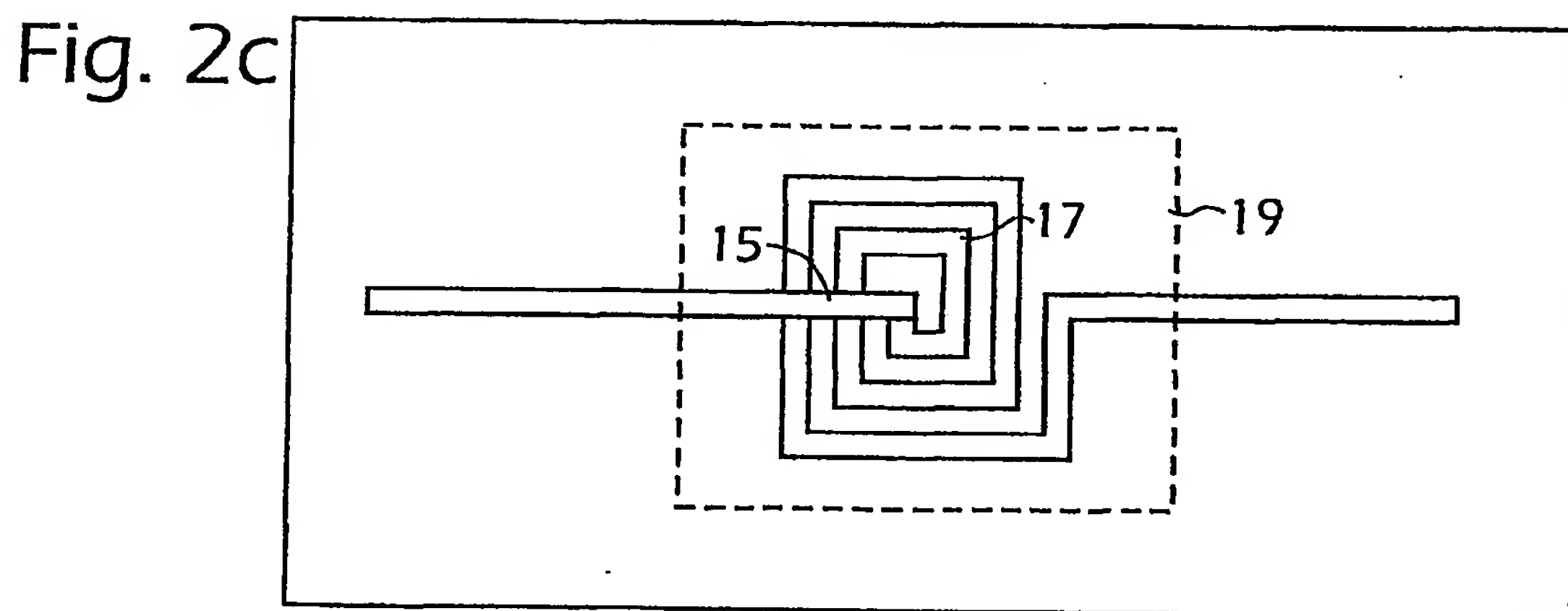
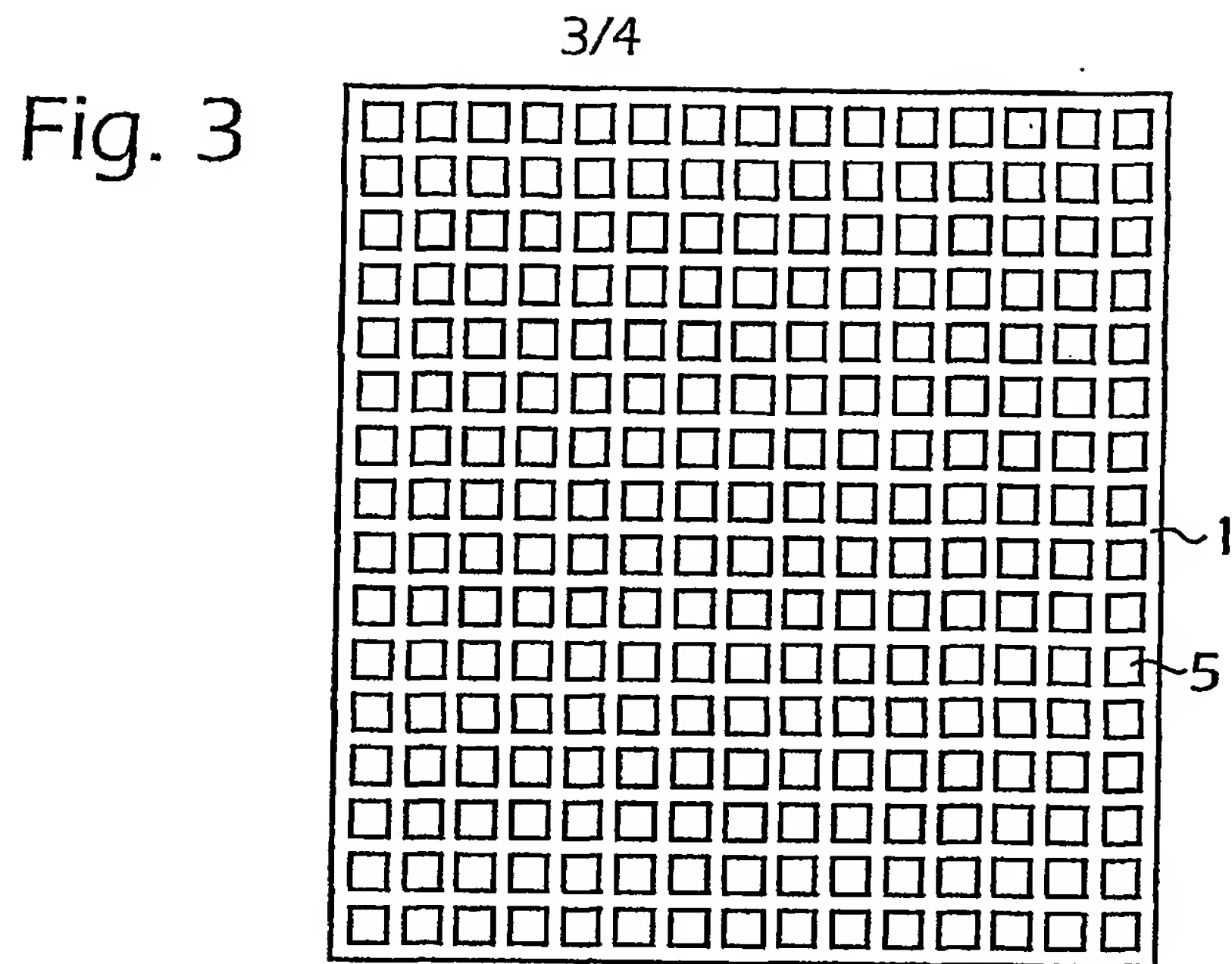


Fig. 2b

Fig. 2a





INTERNATIONAL SEARCH REPORT

International application No.

PCT/SE 01/02768

A. CLASSIFICATION OF SUBJECT MATTER

IPC7: H01L 27/04, H01L 23/60, H01L 23/64

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols).

IPC7: H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-INTERNAL, WPI DATA, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6140197 A (SHAU-FU SANFORD CHU ET AL), 31 October 2000 (31.10.00), column 2, line 66 - column 3, line 24 --	1-12
A	US 6057202 A (TZONG-LIANG CHEN ET AL), 2 May 2000 (02.05.00), column 1, line 41 - line 67, claim 1 --	1-12
A	WO 0067320 A2 (SILICON WAVE, INC.), 9 November 2000 (09.11.00), see the whole document ---	1-12
A	Patent Abstracts of Japan, abstract of JP 11-145386 A (MATSUSHITA ELECTRON CORP.), 28 May 1999 (28.05.99), see abstract --	1-12

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

13 March 2002

Date of mailing of the international search report

18-03-2002

Name and mailing address of the ISA/

Swedish Patent Office

Box 5055, S-102 42 STOCKHOLM

Facsimile No. +46 8 666 02 86

Authorized officer

Fredrik Wahlin/MN

Telephone No. +46 8 782 25 00

INTERNATIONAL SEARCH REPORT

Information on patent family members

28/01/02

International application No.

PCT/SE 01/02768

Patent document cited in search report			Publication date	Patent family member(s)	Publication date
US	6140197	A	31/10/00	EP 1081763 A	07/03/01
US	6057202	A	02/05/00	NONE	
WO	0067320	A2	09/11/00	AU 4812800 A	17/11/00
				US 6310387 B	30/10/01